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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,229	03/03/2004	Larry D. Kinsman	4585.3US (00-0658.03/US)	4782

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,229	KINSMAN, LARRY D.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 01/20/2006 has been reviewed and placed of record in the file.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "plurality of openings extending proximate more than one side of a periphery of the substrate" in "the at least one opening of the substrate of the at least one semiconductor assembly comprises a plurality of openings extending proximate more than one side of a periphery of the substrate" of claim 16 - wherein said at least one opening of said substrate appears to derive antecedent basis from said at least one substantially centrally located opening as recited in claim 1 - and the "extends proximate more than one side of a periphery of the substrate" in "the at least one opening of the substrate of the at least one semiconductor assembly extends proximate more than one side of a periphery of the substrate" of claim 17 - wherein said at least one opening of said substrate appears to derive antecedent basis from said at least one substantially centrally located opening as recited in claim 1 - must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Response to Arguments

3. Applicant's arguments with respect to amended claims 1-24, filed 01/20/2006, have been considered but they are not persuasive and they are moot in view of new ground(s) of rejection.

Allowable Subject Matter

4. The indicated allowability of claims 16 and 18 is withdrawn in view of the 112-section rejection, detailed below or next page.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

5. **Claims 16-18** are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites: "wherein the at least one opening of the substrate of the at least one semiconductor assembly comprises a plurality of openings extending proximate more than one side of a periphery of the substrate" wherein said at least one opening of said substrate appears to derive antecedent basis from said at least one substantially centrally located opening as recited in claim 1. It is not clear, therefore not distinct and indefinite, as to the degree of "substantially centrally located" and said substantially centrally located opening "extending proximate more than one side of a periphery" because the limitation periphery conventionally does convey the meaning of not being central.

Claim 17 is not distinct for substantially the same reason as given for claim 16.

Claim 18 depends from rejected claim 16 and includes all limitations of claim 16 thereby rendering the claim indefinite.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 1-10, 14, and 19-24** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ball U.S. Patent 5,917,242 (cited by Applicant, and hereinafter referred to as the '242 reference).

Referring to **claims 1-4, 14, and 19-24**, the '242 reference discloses in the figures, particularly Fig. 1, and respective portions of the specification a semiconductor assembly substantially as claimed including an opening or at least one opening but does not teach that the semiconductor assembly could be used in a computer system. The reference further does not disclose in words that the at least one opening is substantially centrally located.

Specifically, the reference teaches a semiconductor assembly comprising:

a substrate (14, "leadframe or other conductor-carrying substrate 14, column 5, lines 50-55) having a first surface, a second surface and at least one opening (no number) therethrough, said at least one opening in said substrate extending from said first surface to said second surface of said substrate;

a semiconductor die (12) having an active surface and a back surface, said active surface of said semiconductor die attached to said first surface of said substrate;

a plurality of bond wires (28, only one is shown, column 6, first paragraph) extending through said at least one opening in said substrate and bonded from said active surface of said semiconductor die to said second surface of said substrate; and

a plurality of conductive bumps (18, column 5, lines 50-57) disposed between said active surface of said semiconductor die and said first surface of said substrate.

However, as noted above, the reference does not teach that the semiconductor assembly could be used in a computer system. Nevertheless, the reference also particularly fails to exclude such usage, namely utilizing the semiconductor assembly in a computer system, therefore such utilization would have been obvious to one of ordinary skill in the art at the time the invention was made. Such utilization would also require adding necessary and known and available

components such as a printer circuit board, a processor (in re **claim 2**), an input device (in re **claims 3 and 20**), and an output device (in re **claims 4 and 21**).

In addition, as noted above, the reference also does not disclose in words that the at least one opening is substantially centrally located. Nevertheless, the limitation "substantially centrally located" in ""substantially centrally located opening" is interpreted to be obvious to one of ordinary skill in the art at the time the invention was made because at least one of the following two reasons:

ctr1. As noted, the reference does not disclose in words that the at least one opening of the substrate is substantially centrally located in the substrate. However, said at least one opening appears to be substantially centrally located because (ctr1.1): from the figures, for example from Fig. 1, it appears that said at least one opening is substantially centrally located; and (ctr1.2): the reference does not appear to teach that the opening should not be located in a central region of the substrate;

ctr2. Applicant has presented no discussion in the specification which convinces the examiner that the particular position of the substrate opening, i.e., the opening is a substantially centrally located opening, is anything more than one of numerous positions a person of ordinary skill in the art would find obvious for the purpose of providing opening for said substrate. Although the device of the '242 reference does not teach in words the exact location of the opening as that claimed by Applicant, the location differences are considered obvious and are not patentable unless unobvious or unexpected results are obtained from these changes. As a matter of fact, Applicant appears to teach that various locations of said opening of said substrate are a matter of design choice (present invention, paragraphs [0030] and [0041], and design choice was

still generally considered routine skill, at the time the invention was made, of one of ordinary skill in the art.

Referring to **claim 5**, the reference further discloses a filler material (32) located between said semiconductor die and said substrate.

Referring to **claims 6-8**, as the reference does not particularly point out which bond wires or conductive bumps are for power, ground, or signal routing, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the various usage as claimed.

Referring to **claims 9 and 10**, the reference further discloses a sealant material as claimed (column 6, lines 9-16, and column 1, lines 35-40 for a definition of a glob top).

7. **Claims 11-12** are rejected under 35 U.S.C. §103(a) as being unpatentable over Ball U.S. Patent 5,917,242 (cited by Applicant, the '242 reference) as applied above for claim 1 and further in view of Fritz U.S. Patent 5,744,383.

The '242 reference discloses at least one semiconductor assembly that would be easy to be used in a computer system as claimed and as detailed above for claim 1, but does not teach that said at least one semiconductor assembly further comprises interconnect bumps disposed on said second surface of said substrate 14. To be specific, the reference does not - although mentions that said substrate could be any conductor-carrying substrate as noted above - teach that substrate the substrate is a TAB carrier. Instead, as mentioned above, the reference discloses that the substrate is a leadframe.

Fritz, in disclosing a semiconductor device including a semiconductor die, teaches that sophisticated carriers such as a TAB carrier offer more electrical connections to the semiconductor die than a simple leadframe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '242 reference's device such that the substrate is a sophisticated carrier such as a TAB carrier rather than a simple leadframe (column 1, lines 40-45). One would have been motivated to make such a change in view of the teachings in Fritz that such a change offers more electrical connections to the semiconductor die. Such a change, namely using a sophisticated carrier such as a TAB carrier rather than a simple leadframe, would produce the limitation interconnect bumps disposed on said second surface of said substrate, and would require a circuit board (in re claim 12) to function (see, for example, Lee et al. U.S. Patent 6,081,037, Fig. 4).

8. **Claim 13** is rejected under 35 U.S.C. §103(a) as being unpatentable over Ball U.S. Patent 5,917,242 (cited by Applicant, "the '242 reference") in view of Fritz U.S. Patent 5,744,383 as applied above for claim 12 and further in view of Chiu U.S. Patent 6,228,679.

The '242 reference modified in view of Fritz discloses a device as claimed and as detailed above for claim 12, but fails to teach a filler material between said second surface of said substrate and said circuit board.

Chiu, in disclosing a semiconductor device including a semiconductor die, a substrate and a circuit board, teaches a simple method of dispersing underfill materials under the semiconductor die (column 2, lines 10-20), and further teaches dispersing the underfill materials

also between a second surface of said substrate and said circuit board (column 1, lines 45-54) so as to obtain mechanical integrity and reliability for the device (column 1, lines 22-30).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '242 reference's device in view of Fritz such that it includes an underfill materials between a second surface of said substrate and said circuit board. One would have been motivated to make such a change in view of the teachings in Chiu that such a change produces mechanical integrity and reliability for the device.

9. **Claim 15** is rejected under 35 U.S.C. §103(a) as being unpatentable over Ball U.S. Patent 5,917,242 (cited by Applicant, "the '242 reference"), further in view of Fritz U.S. Patent 5,744,383, and further in view of Jiang U.S. Patent 6,011,307

The '242 reference discloses at least one semiconductor assembly that would be easy to be used in a computer system as claimed and as detailed above for claim 14, but does not teach that said at least one semiconductor assembly further comprises interconnect bumps disposed on said second surface of said substrate 14. To be specific, the reference does not, although mentions that said substrate could be any conductor-carrying substrate as noted above, teach that substrate the substrate is a TAB carrier or other advanced substrate carriers. Instead, as mentioned above, the reference discloses that the substrate is a leadframe.

Fritz, in disclosing a semiconductor device including a semiconductor die, teaches that sophisticated carriers such as a TAB carrier offer more electrical connections to the semiconductor die than a simple leadframe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '242 reference's device

such that the substrate is a sophisticated carrier such as a TAB carrier rather than a simple leadframe (column 1, lines 40-45). One would have been motivated to make such a change in view of the teachings in Fritz that such a change offers more electrical connections to the semiconductor die. Such a change, namely using a sophisticated carrier such as a TAB carrier rather than a simple leadframe, would produce the limitation interconnect bumps disposed on said second surface of said substrate, and would require a circuit board (in re claim 12) to function (see, for example, Lee et al. U.S. Patent 6,081,037, Fig. 4).

Such a modification in view of Fritz would produce a semiconductor device wherein said semiconductor die is attached to said substrate having centrally located bond pads (26, the '242 reference) on said active surface of said semiconductor die exposed through said at least one opening. Such modification also produces outer bond pads (20, the '242 reference) on said active surface of said semiconductor die. However, the teachings do not disclose that said outer bond pads (20, the '242 reference) on said active surface of said semiconductor die are mirrored with bond pads on said first surface of said substrate having said plurality of conductive bumps therebetween. In other words, the references do not teach that for every connecting bump there are two corresponding bond pads one on the active surface of the semiconductor die and the other on the first surface of the substrate that are in mirrored relationship.

Jiang, in disclosing a semiconductor device including a semiconductor die and a circuit board, teaches that the connection between the semiconductor die and the circuit board requires connection pads on both sides of the two elements that are to be connected to each other and that the connection pads are mirrored (column 1, lines 30-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '242 reference's

device such that it includes connection pads on both sides of the two elements that are to be connected to each other, in the present case the semiconductor die and the substrate carrier, and that the connection pads on the respective elements are mirrored to each other. One would have been motivated to make such a change in view of the teachings in Jiang that such a change is required for the resulting structure to function.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 27, 2006